

ABSTRACT OF THE DISCLOSURE

A logic circuit block and a memory circuit block are provided on a semiconductor chip. A timing adjustment circuit block for adjusting the propagation timing of signals is provided on a line between the circuit blocks. A timing adjustment circuit unit includes: a
5 delay element block including a plurality of delay elements for adding different delay amounts to the inter-block signals; a counter circuit block for receiving a timing adjustment control signal from the timing adjustment circuit block; and a fuse circuit block in which a fuse is melted down based on a fuse information signal held by the counter
10 circuit block after a timing verification and which replaces the function of the counter circuit block.